Amendments to th claims:

Claims 1-10: (canceled)

11. (currently amended) A circuit arrangement for controlling a starting relay of a starter for a motor vehicle internal combustion engine, comprising,

a battery (20), wherein said battery is electrically connected to the starting relay (4);

a computer (19) that is disposed in the control circuit of the starting relay (4), wherein between the computer (19) and the starting relay (4), a memory circuit (2) is disposed, wherein said memory circuit is embodied to maintain the existing control signal (STEN) for the starting relay (4) during a chronologically limited undervoltage of the battery (20), wherein between the computer (19) and the memory circuit (2), a locking circuit (1) is disposed, and wherein the locking circuit (1) detects the instantaneous logic state at a control input (STEN) and stores it in memory with the aid of the memory circuit (2).

12. (previously amended) The circuit arrangement of claim 11, wherein the memory circuit (2) has a flip-flop (14, 15).

13. (previously amended) The circuit arrangement of claim 12, wherein the flip-flop (14, 15) is settable by means of an RC circuit (17, 18) in

such a way that the starting relay (4) is set to the inactive state upon reapplication of the battery voltage.

14. (canceled)

15. (canceled)

16. (currently amended) The circuit arrangement of claim ~~14~~ 11, wherein the locking circuit (1) is embodied to maintain the triggering for the starting relay (4) if the computer (19) is in a reset mode.

17. (currently amended) The circuit arrangement of claim ~~14~~ 11, wherein the computer (19) switches the locking circuit (1) to be inactive once the undervoltage of the battery (20) is ended.

18. (previously amended) The circuit arrangement of claim 11, wherein the computer (19) has a program with which the locking circuit (1) and/or the memory circuit (2) can be controlled.

19. (previously amended) The circuit arrangement of claim 11, wherein the locking circuit and memory circuit (1, 2) span a voltage dip down to approximately 0 volts.

20. (previously amended) The circuit arrangement of claim 19, wherein voltages up to approximately 4 volts can be spanned without chronological limitation, and voltages under 4 volts can be spanned with chronological limitation.